Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently amended) A memory chip comprising a substrate, into which memory cells are introduced,

the memory cells having a trench capacitor and a transistor,

the trench capacitor at least partially having a filling, and

the transistor having a source terminal, a drain terminal and a gate terminal,

the drain terminal being electrically conductively connected to the trench capacitor, wherein

the filling at least partially has a material which is unstable at high temperatures, which occur during a high-temperature process during fabrication of the memory chip, the filling being introduced after the high-temperature processes, and the filling not exposed to a high-temperature process, wherein the filling has at least one of the materials from the following group: hafnium oxide, lanthanum oxide and yttrium oxide.

2. (Canceled)

3. (Currently amended) The memory chip as claimed in claim [[2]]1, wherein the filling has a silicate compound.

4. (Previously presented) The memory chip as claimed in claim 1, wherein the filling at least partially has a metallic material.

5. (Currently amended) The memory chip as claimed in claim 1, wherein

a wall of the trench is at least partially covered with a dielectric layer,

a metallic layer is at least partially applied on the dielectric layer, and

the metallic layer is electrically conductively connected to the drain terminal of the transistor via a strap filling.

6. (Previously presented) The memory chip as claimed in claim 1, wherein an electrically conductive layer is formed in a manner adjoining the trench in the substrate.

7. (Currently amended) The memory chip as claimed in claim 1, wherein

the trench is covered by an epitaxial layer,

an opening is introduced in the epitaxial layer,

a conductive connection between the filling and the drain terminal is formed through the opening, and

a dielectric layer is at least partially applied on a side of the epitaxial layer which faces the trench.

8. (Currently amended) The memory chip as claimed in claim 1, wherein the memory chip is fabricated by the method comprising:

introducing a trench into a substrate;

filling the trench at least partially with a dummy filling;

applying a covering layer to the substrate~~, which covering layer is formed as an epitaxial layer~~;

introducing a transistor into the covering layer;

removing the dummy filling from the trench;

introducing a storage dielectric and a trench electrode into the trench, a trench capacitor being created, and

forming a connection of the trench electrode to a terminal of the transistor.

9. (Withdrawn) The method as claimed in claim 8, wherein a channel is etched into the covering layer as far as the dummy filling,

the dummy filling is etched out via the channel,

a dielectric layer is at least partially applied to the wall of the trench,

a conductive layer is applied to the dielectric layer, and

the conductive layer is electrically conductively connected to a terminal of the transistor.

10. (Withdrawn) The method as claimed in claim 8, wherein, after the etching of the channel, sidewalls of the channel are covered with a protective layer made of nitride, and the dummy filling is subsequently etched out from the trench.